We claim:

1. A device for a bidirectional transfer of data, comprising:

a first processor;

a second processor;

an input memory connected to said second processor, said input memory having a plurality of memory blocks for receiving output data from said first processor;

an output memory with a plurality of memory blocks for providing input data for said first processor, said output memory connected to said second processor;

an input control information memory connected to said input memory and storing an item of binary control information for each of said memory blocks of said input memory;

an output control information memory connected to said output memory and storing an item of binary control information for each of said memory blocks of said output memory; and

at least one direct memory access (DMA) channel for writing the output data from said first processor to said input memory and for reading the input data for said first processor from

said output memory, said DMA channel connected to said first processor, said input memory and said output memory, access to said input memory and said output memory being regulated such that a write access of said first processor and a read access of said second processor to said input memory is permitted on a basis of the item of control information stored in said input control information memory, and the write access of said second processor and the read access of said first processor to said output memory is permitted on a basis of the item of control information stored in said output control information memory.

2. The device according to claim 1, wherein a write access operation of said first processor to a memory block of said input memory is permitted only if the item of binary control information for the memory block is in a first state.

3. The device according to claim 2, wherein a read access operation of said second processor to the memory block of said input memory is permitted only if the item of binary control information for the memory block is in a second state.

4. The device according to claim 1, wherein a read access operation of said first processor to a memory block of said output memory is permitted only if the item of binary control information for the memory block is in a first state.

5. The device according to claim 4, wherein a write access operation of said second processor to a memory block of said output memory is permitted only if the item of binary control information for the memory block is in a second state.

6. The device according to claim 1, wherein if said output memory and said input memory have different memory sizes, a number of the memory blocks is identical in both of said output memory and said input memory.

7. The device according to claim 1, wherein at least one of said input memory and said output memory are cyclic memories.

8. The device according to claim 1, wherein said first processor is a digital signal processor, and said second processor is a hardware logic circuit.

9. A turbo decoder for a mobile radio receiver, comprising:

a device for a bidirectional transfer of data, including:

a processor being a digital signal processor;

a decoder being a hardware logic circuit;

an input memory connected to said decoder, said input memory having a plurality of memory blocks for receiving output data from said processor;

an output memory with a plurality of memory blocks for providing input data for said processor, said output memory connected to said decoder;

an input control information memory connected to said decoder and storing an item of binary control information for each of said memory blocks of said input memory;

an output control information memory connected to said decoder and storing an item of binary control information for each of said memory blocks of said output memory; and

at least one direct memory access (DMA) channel for writing the output data from said processor to said input memory and for reading the input data for said processor from said output memory, said DMA channel connected to said processor, said input control information memory and said output control information memory, access to said input memory and said output memory being regulated such that a write access of said processor and a read access of said decoder to said input memory is permitted on a basis of the item of control information stored in said

input control information memory, and the write access of said decoder and the read access of said processor to said output memory is permitted on a basis of the item of control information stored in said output control information memory.

10. A method for a bidirectional transfer of data, which comprises the steps of:

providing a first processor, a second processor, an input memory connected to the second processor and having a plurality of memory blocks for receiving output data from the first processor, an output memory connected to the second processor and having a plurality of memory blocks for providing input data for the first processor, an input control information memory storing an item of binary control information for each of the memory blocks of the input memory, and an output control information memory storing an item of binary control information for each of the memory blocks of the output memory;

permitting a write access operation, taking place through a direct memory access (DMA) channel, of the first processor and a read access operation of the second processor to the input memory on a basis of the item of control information stored in the input control information memory; and

permitting the write access operation of the second processor and the read access operation, taking place through the DMA channel, of the first processor to the output memory on a basis of the item of control information stored in the output control information memory.

11. A device for a bidirectional transfer of data between a first processor and a second processor, the second processor having an input memory with a plurality of memory blocks for receiving output data from the first processor and an output memory with a plurality of memory blocks for providing input data for the first processor, the device comprising:

an input control information memory connected to the input memory and storing an item of binary control information for each of the memory blocks of the input memory;

an output control information memory connected to the output memory and storing an item of binary control information for each of the memory blocks of the output memory; and

at least one direct memory access (DMA) channel for writing the output data from the first processor to the input memory and for reading the input data for the first processor from the output memory, said DMA channel connected to the first

processor, the input memory and the output memory, access to the input memory and the output memory being regulated such that a write access of the first processor and a read access of the second processor to the input memory is permitted on a basis of the item of control information stored in said input control information memory, and the write access of the second processor and the read access of the first processor to the output memory is permitted on a basis of the item of control information stored in the output control information memory.